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EXAMINER	
ETTEHADIEH, ASLAN	
ART UNIT	**PAPER NUMBER**
2637	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/874,310	CHIBA, KENICHIRO	
	Examiner	Art Unit	
	Aslan Ettehadieh	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 25, 28, 29* is/are rejected.

7)☒ Claim(s) *26, 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/8/03, 12/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification is objected to minor informalities:

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The word "For" has been misspelled as "Foe" (page 12 line 15).

4. The word "combating" has been misspelled as "combatting" (page 1 line 25 and page 2 line1)

5. The word "synthesizing" has been misspelled as "synthesising" (page 6 line 25).

6. The word "the" has been misspelled as "th" (page 8 line 13 and page 15 line 19).

Appropriate correction is required.

Claim Objections

7. Claims 24 – 27 are objected to because of the following informalities: the phases in brackets should be deleted because they are not given patentable weight.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 7 is contradictory. Page 4 line 7 reads not including a delay lock loop circuit and page 4 line 9 reads but including a sole DLL.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3, 5, 7, 10, 11, 12, 14,15, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 6266365) in view of Miura (US 6658046).

10. Regarding claim 1, Wang discloses a RAKE reception apparatus (col 4 lines 6 – 7) having a delay lock loop circuit, termed "DLL circuit" (col 4 lines 10 – 12), herein, for performing control to keep synchronization for a plurality of finger circuits adapted for separately despreading and demodulating reception signals passed through respective paths of the multiple paths (col 4 lines 20 – 28), said apparatus comprising: synchronous tracking in said DLL circuit (col 4 lines 40 – 47) based on the information at the time of output synthesis in a RAKE combiner adapted for combining outputs of said plural circuits with output demodulated signals (col 4 lines 47 – 49); and means for aligning the phase of said DLL circuit with the phase of the selected one finger circuit (col 4 lines 49 – 51, col 5 lines 50 – 54, and col 6 lines 19 – 39). However, Wang does not disclose a means for selecting one of the finger circuits.

In the same field of endeavor, however, Miura discloses a means for selecting one of the finger circuits (col 1 lines 36 – 37).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use a means for selecting one of the finger circuits as taught by

Miura in the system of Wang's RAKE reception apparatus in order to provide for much higher traffic density thus providing better efficiency.

11. Regarding claim 3, Wang discloses all limitations of claim 3 as analyzed in claim 1 above. Wang further discloses a RAKE reception apparatus wherein said DLL circuit includes means for detecting the correlation between a reference signal leading and lagging an optimal phase each by a preset timing, and a reception signal, (col 4 lines 25 – 28 and col 6 lines 19 – 29)) and for varying the oscillation frequency of clocks (figure 1 element 800) based on the difference information of outputs of the correlation values, (col 4 lines 48 – 51) said clocks (figure 1 element 800) being supplied to a pseudorandom noise PN sequence generator (figure 2 element 24) in said DLL circuit adapted for generating said leading and lagging reference signals and to said plural finger circuits; (col 6 lines 19 –27) and wherein the selected one of the finger circuits in said DLL circuit to align a code phase of said DLL circuit with a code phase of the selected one finger circuit (col 4 lines 46 – 51). However, Wang does not disclose a shift register value of the PN sequence generator is loaded in a shift register of the PN sequence generator.

In the same field of endeavor, however, Miura discloses a shift register value of the PN sequence generator (figure 1 element 108) is loaded in a shift register (figure 1element 110) of the PN sequence generator.

Therefore it would have been obvious to one skilled in the art at the time of invention was made to have a shift register value of the PN sequence generator is loaded in a shift register of the PN sequence generator as taught by Miura in the system

of Wang's RAKE reception apparatus to ensure a quick search of the rake finger in order to provide more efficient processing time (col 1 lines 14 – 30).

12. Regarding claim 5, Wang discloses all limitations of claim 5 as analyzed in claim 1 above. Wang further discloses a RAKE reception apparatus wherein said DLL circuit includes means for detecting the correlation between reference signals leading and lagging an optimal phase each by a preset timing, and a reception signal (col 4 lines 25 – 28), and means for varying the oscillation frequency of clocks based on the difference information of outputs of the correlation values (col 4 lines 48 – 51); said clocks (figure 2 element 24) being supplied to said plural finger circuits (figure 2 element 9), and said DLL circuit being not provided with PN sequence generators (Figure 2 elements 9, 22 and 24, where element 9 is being provided to element 22 and not element 24); said DLL circuit being fed with a reference signal leading and lagging a preset timing with respect to an optimal phase (col 6 lines 29 – 32, where early is interpreted as leading and late being interpreted as lagging), said reference signal being output by the PN sequence generator of the selected one of the finger circuits (figure 2 elements 22 and 24), said DLL circuit using these reference signals for detecting the correlation with respect to the reception signal to align the code phase of said DLL circuit with the code phase of the selected one of the finger circuits (col 6 lines 19 – col 7 line 7).

13. Regarding claim 7, Wang discloses a RAKE reception apparatus (col 4 lines 6 – 7) including: a plurality of finger circuits (col 5 line 62) for despreading and demodulating respective reception signals (col 4 lines 64 – 65) retrieved by a searcher adapted for retrieving respective paths from multipath reception signals (col 4 lines 3 – 17), and a

RAKE combiner for combining demodulated outputs from said plural finger circuits (col 4 lines 3 – 9), said plural finger circuits not including a delay lock loop circuit termed "DLL circuit", for synchronization holding controlling in its inside, but including a sole DLL circuit in common for said plural finger circuits (figure 2 element 22); said RAKE reception apparatus comprising: a circuit that said plural finger circuits to be synchronization tracked by said DLL circuit among the plural finger circuits (col 1 lines 32 – 43); and a control circuit for receiving the finger-circuit-based information (col 4 lines 10 – 15) used by said RAKE combiner in combining outputs of said finger circuits (col 6 lines 6 – 9), said one of the finger circuits to be tracked by said DLL circuit, based on said information (col 1 lines 38 – 41). However, Wang does not disclose a changeover circuit for switching to one said plural finger among the plural finger circuits and selecting said one of the finger circuits for commanding the switching to said changeover circuit.

In the same field of endeavor, however, Miura discloses a means for a changeover circuit for switching to one said plural finger among the plural finger circuits and selecting said one of the finger circuits for commanding the switching to said changeover circuit (col 1 lines 31 – 43).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use a means for a changeover circuit for switching to one said plural finger among the plural finger circuits and selecting said one of the finger circuits for commanding the switching to said changeover circuit as taught by Miura in the

system of Wang's RAKE reception apparatus to establish synchronization in a shorter period of time in order to provide more efficiency in the processing time.

14. Regarding claim 10, Wang discloses all limitations of claim 10 as analyzed in claim 1 above. Wang further discloses a RAKE reception apparatus wherein clocks output from said DLL circuit (col 1 lines 48 – 51) are routed not only to the one of the plural finger circuits selected by said changeover circuit but also to the remaining finger circuits (col 1 lines 51 – 56).

15. Regarding claim 11, Wang discloses all limitations of claim 11 as analyzed in claim 10 above. Wang further discloses a RAKE reception apparatus wherein said clocks output from said DLL circuit are routed to the PN sequence generator (figure 2 element 24) of each finger circuit to perform synchronization holding operation (col 1 lines 32 – 54).

16. Regarding claim 12, Wang discloses all limitations of claim 12 as analyzed in claim 7 above. Wang further discloses a RAKE reception apparatus wherein said DLL circuit receives an output signal and based on the received signal aligns the phase (col 1 lines 34 – 43). Miura further discloses of the one finger circuit selected by said changeover circuit and, based on the received signal, aligns the phase of the pseudorandom noise, termed "PN", code used for despreading the received data with the phase of the PN sequence generator in said one finger circuit selected by said changeover circuit (aligning is done by figure 1 elements 104, 106, and 110).

17. Regarding claim 14, Wang in discloses all limitations of claim 14 as analyzed in claim 7 above. Wang further discloses a RAKE reception apparatus wherein the phase

of the PN sequence generator in said DLL circuit is aligned to the phase of the PN sequence generator in the one finger circuit (col 4 lines 49 – 51, col 5 lines 50 – 54, and col 6 lines 19 – 39). Miura discloses that one finger circuit selected by said changeover circuit (col 1 lines 31 – 43).

18. Regarding claim 15, Wang discloses all limitations of claim 15 as analyzed in claim 7 above. Miura further discloses a RAKE reception apparatus (figure 1) wherein the value of the shift register (figure 1 element 107 and 110) constituting the PN sequence generator (figure 1 element 108) of the selected (col 1 lines 35 – 40) one of the plural finger circuits (figure 1 plural elements 101) is routed through said changeover circuit to said DLL (figure 1 element 104, where element 104 is interpreted as Wang's DLL control structure) circuit (col 3 lines 58 – 67) and wherein the value of the shift register constituting the PN sequence generator in said DLL circuit is set to a value of the shift register input through said changeover circuit (col 3 lines 58 – 67) to align the phase of the PN sequence generator in said DLL circuit with the phase of the PN sequence generator in the selected one of the finger circuits (where aligning is done by figure 1 elements 104, 106, and 110).

19. Regarding claim 28, Wang discloses all limitations of claim 28 as analyzed in claim 1 above. Wang further discloses a RAKE reception apparatus wherein one or a plurality of said DLL circuits are provided each one of which is provided in each group of a plurality of finger circuits (figure 2 elements 9 and 22).

20. Regarding claim 29, Wang discloses all limitations of claim 29 as analyzed in claim 7 above. Wang further discloses a RAKE reception apparatus wherein one or a

plurality of said DLL circuits are provided each one of which is provided in each group of a plurality of finger circuits (figure 2 elements 9 and 22).

21. Claims 2, 4, 6, 8, 9, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 6266365) in view of Miura (US 6658046) and in further view of Schmidl (US 6816541).

22. Regarding claim 2, Wang in discloses all limitations of claim 2 as analyzed in claim 1 above. However, Wang does not disclose at the time of maximum ratio combining in said RAKE combiner, the finger circuit on which the maximum weighting is placed is selected based on the weighting information afforded to an output of said finger circuit.

In the same field of endeavor, however, Schmidl discloses at the time of maximum ratio combining in said RAKE combiner, the finger circuit on which the maximum weighting is placed is selected based on the weighting information afforded to an output of said finger circuit (col 1 lines 56 – 64).

Therefore it would have been obvious to one skilled in the art at the time of invention was made that at the time of maximum ratio combining in said RAKE combiner, the finger circuit on which the maximum weighting is placed is selected based on the weighting information afforded to an output of said finger circuit as taught by Schmidl in the system of Wang RAKE reception apparatus to improve signal to noise ratio to provide a cleaner signal.

23. Regarding claim 4, Wang discloses all limitations of claim 4 as analyzed in claim 2 above. Wang further discloses a RAKE reception apparatus wherein said DLL circuit

includes means for detecting the correlation between a reference signal leading and lagging an optimal phase each by a preset timing, and a reception signal, (col 4lines 25 – 28) and for varying the oscillation frequency of clocks (figure 1 element 800) based on the difference information of outputs of the correlation values, (col 4 lines 48 – 51) said clocks (figure 1 element 800) being supplied to said DLL circuit adapted for generating said leading and lagging reference signals and to said plural finger circuits; (col 6 lines 19 –27) and wherein the selected one of the finger circuits in said DLL circuit to align a code phase of said DLL circuit with a code phase of the selected one finger circuit (col 4 lines 46 – 51). However, Wang does not disclose a pseudorandom noise PN sequence generator and a shift register value of the PN sequence generator is loaded in a shift register of the PN sequence generator.

In the same field of endeavor, however, Miura discloses a pseudorandom noise PN sequence generator (figure 1 element 108) and a shift register value of the PN sequence generator is loaded in a shift register (figure 1element 110) of the PN sequence generator.

Therefore it would have been obvious to one skilled in the art at the time of invention was made to have a pseudorandom noise PN sequence generator and a shift register value of the PN sequence generator is loaded in a shift register of the PN sequence generator as taught by Miura in the system of Wang's RAKE reception apparatus to ensure a quick search of the rake finger in order to provide more efficient processing time (col 1 lines 14 – 30).

24. Regarding claim 6, Wang discloses all limitations of claim 6 as analyzed in claim 2 above. Wang further discloses a RAKE reception apparatus wherein said DLL circuit includes means for detecting the correlation between reference signals leading and lagging an optimal phase each by a preset timing, and a reception signal (col 4 lines 25 – 28), and means for varying the oscillation frequency of clocks based on the difference information of outputs of the correlation values (col 4 lines 48 – 51); said clocks (figure 2 element 24) being supplied to said plural finger circuits (figure 2 element 9), and said DLL circuit being not provided with PN sequence generators (Figure 2 elements 9, 22 and 24, where element 9 is being provided to element 22 and not element 24); said DLL circuit being fed with a reference signal leading and lagging a preset timing with respect to an optimal phase (col 6 lines 29 – 32, where early is interpreted as leading and late being interpreted as lagging), said reference signal being output by the PN sequence generator of the selected one of the finger circuits (figure 2 elements 22 and 24), said DLL circuit using these reference signals for detecting the correlation with respect to the reception signal to align the code phase of said DLL circuit with the code phase of the selected one of the finger circuits (col 6 lines 19 – col 7 line 7).

25. Regarding claim 8, Wang discloses all limitations of claim 8 as analyzed in claim 7 above. Wang further discloses a RAKE reception apparatus wherein the DLL circuit to track the optimal finger circuit (col 1 lines 34 – 43 and 48 – 56). Miura further discloses a RAKE reception apparatus (figure 1) wherein said control circuit (figure 1 element 22) selects the finger circuit, for which said control circuit commanding said changeover circuit to effect the switching (col 1 lines 34 – 40 and col 2 lines 31 – 49)

based on the information output by said RAKE combiner (col 1 lines 62 – 67). However Wang does not disclose the maximum weighting is put, based on the finger-circuit-based weighting information.

In the same field of endeavor, however, Schmidl discloses the maximum weighting is put, based on the finger-circuit-based weighting information (col 1 lines 56 – 64).

Therefore it would have been obvious to one skilled in the art at the time of invention was made that the maximum weighting is put, based on the finger-circuit-based weighting information as taught by Schmidl in the system of Wang RAKE reception apparatus to improve signal to noise ratio to provide a cleaner signal.

26. Regarding claim 9, Wang discloses all limitations of claim 9 as analyzed in claim 8 above. Schmidl further discloses a RAKE reception apparatus wherein said RAKE combiner combines the demodulated signals output by each finger circuit by a maximal ratio combining method. (col 1 lines 56 – 64).

27. Regarding claim 13, Wang discloses all limitations of claim 13 as analyzed in claim 7 above. Wang further discloses a RAKE reception apparatus wherein said DLL circuit receives an output signal and, based on the received signal, aligns the phase (col 1 lines 34 – 43), wherein the DLL circuit to track the optimal finger circuit (col 1 lines 34 – 43 and 48 – 56), wherein clocks output from said DLL circuit (col 1 lines 48 – 51) are routed not only to the one of the plural finger circuits selected by said changeover circuit but also to the remaining finger circuits (col 1 lines 51 – 56); a RAKE reception

apparatus wherein said clocks output from said DLL circuit are routed to each finger circuit to perform synchronization holding operation (col 1 lines 32 – 54).

Miura further disclose of the one finger circuit selected by said changeover circuit and, based on the received signal, aligns the phase of the pseudorandom noise, termed "PN", code used for despreading the received data with the phase of the PN sequence generator in said one finger circuit selected by said changeover circuit (aligning is done by figure 1 elements 104, 106 and 110); wherein said control circuit (figure 1 element 22) selects the finger circuit, for which said control circuit commanding said changeover circuit to effect the switching (col 1 lines 34 – 40 and col 2 lines 31 – 49) based on the information output by said RAKE combiner (col 1 lines 62 – 67); also, the output from said DLL circuit are routed to the PN sequence generator (figure 1 elements 104 and 108, where element 104 is interpreted as Wang's DLL control structure).

However Wang does not disclose the maximum weighting is put, based on the finger-circuit-based weighting information and wherein said RAKE combiner combines the demodulated signals output by each finger circuit by a maximal ratio combining method.

In the same field of endeavor, however, Schmidl discloses the maximum weighting is put, based on the finger-circuit-based weighting information (col 1 lines 56 – 64) and a RAKE reception apparatus wherein said RAKE combiner combines the demodulated signals output by each finger circuit by a maximal ratio combining method. (col 1 lines 56 – 64).

Therefore it would have been obvious to one skilled in the art at the time of invention was made that the maximum weighting is put, based on the finger-circuit-based weighting information and a RAKE reception apparatus wherein said RAKE combiner combines the demodulated signals output by each finger circuit by a maximal ratio combining method. (col 1 lines 56 – 64) as taught by Schmidl in the system of Wang RAKE reception apparatus to improve signal to noise ratio to provide a cleaner signal.

28. Claims 16, 17, 18, 19, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 6266365) in view of Miura (US 6658046) and in further view of Naruse (US 6075809).

29. Regarding claim 16, Wang discloses all limitations of claim 16 as analyzed in claim 7 above. Miura discloses a RAKE reception apparatus (figure 1) wherein the PN code string output by the PN sequence generator (figure 1 element 108) of the selected (col 1 lines 35 – 40) one of the plural finger circuits (figure 1 element 101) is routed through said changeover circuit to said DLL circuit (figure 1 element 104, where element 104 is interpreted as Wang's DLL control structure). However, Wang does not disclose wherein said DLL circuit despreads the reception data using the PN code string output from the PN sequence generator of the selected one finger circuit for phase alignment with respect to the PN sequence generator in the selected one finger circuit.

In the same field of endeavor, however, Naruse discloses wherein said DLL circuit despreads the reception data using the PN code string output from the PN

sequence generator of the selected one finger circuit for phase alignment with respect to the PN sequence generator in the selected one finger circuit (col 16 lines 57 – 67)

Therefore it would have been obvious to one skilled in the art at the time of invention was made that said DLL circuit despreads the reception data using the PN code string output from the PN sequence generator of the selected one finger circuit for phase alignment with respect to the PN sequence generator in the selected one finger circuit as taught by Naruse in the system of Wang RAKE reception apparatus to alleviate the fading due to the multi-paths and to improve signal to noise ratio to provide a cleaner signal.

30. Regarding claim 17, Wang discloses all limitations of claim 17 as analyzed in claim 7 above. Wang further discloses a RAKE reception apparatus wherein said DLL circuit (figure 2 element 22) includes a PN sequence generator (figure 2 element 24) for generating and outputting an early PN code (figure 4B, output of element 60) leading the PN code used in said finger circuit in timing and for generating and outputting a late PN code (figure 4B output of element 62) lagging the PN code used in said finger circuit in timing (col 1 lines 48 – 54 and col 4 lines 46 – 60); a loop filter for smoothing an output of said subtractor (col 5 lines 55 – 58). Miura further discloses a voltage-controlled oscillator fed with an output (figure 1 element 104), a shift register of said PN sequence generator of being loaded with a value of a shift register of the PN sequence generator of the one selected finger circuit through said changeover circuit (figure 1 elements 101, 107, and 108); an output clock of said voltage-controlled oscillator (figure 1 element 104) being supplied to said PN sequence generator (figure 1 element 108) in

said DLL circuit while being fed as a control clock to each of said finger circuits (figure 1 plurality of elements 101). However Wang does not disclose first and second multipliers for multiplying reception data with said early PN code and the late PN code, respectively; first and second filters fed with outputs of said first and second multipliers, respectively; first and second detectors for detecting outputs of said first and second filters, respectively; a subtractor for subtracting an output of said second detector from an output of said first detector; and a voltage-controlled oscillator fed with an output of said loop filter as a control voltage.

In the same field of endeavor, however, Naruse discloses first and second multipliers for multiplying reception data with said early PN code and the late PN code, respectively (figure 6 elements 79, 80, and 81); first and second filters fed with outputs of said first and second multipliers, respectively (figure 6 elements 87 and 88); first and second detectors for detecting outputs of said first and second filters, respectively (figure 6 elements 89 and 90); a subtractor for subtracting an output of said second detector from an output of said first detector (figure 6 element 91); and a voltage-controlled oscillator fed with an output of said loop filter as a control voltage (figure 6 elements 75 and 92, where element 75 is interpreted as Miura's controller).

Therefore it would have been obvious to one skilled in the art at the time of invention was made that a first and second multipliers for multiplying reception data with said early PN code and the late PN code, respectively; first and second filters fed with outputs of said first and second multipliers, respectively; first and second detectors for detecting outputs of said first and second filters, respectively; a subtractor for

subtracting an output of said second detector from an output of said first detector; and a voltage-controlled oscillator fed with an output of said loop filter as a control voltage as taught by Naruse in the system of Wang RAKE reception apparatus to alleviate the fading due to the multi-paths and to improve signal to noise ratio to provide a cleaner signal.

31. Regarding claim 18, Wang discloses all limitations of claim 18 as analyzed in claim 7 above. Miura further discloses a The RAKE reception apparatus wherein a value of the shift register constituting the PN sequence generator of the selected finger circuit is supplied through said changeover circuit to said DLL circuit (col 3 lines 58 – 67). However Wang does not disclose said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code; a multiplier for multiplying input reception data with the PN sequence from said PN sequence generator; and a low-pass filter for smoothing an output of said multiplier to output a demodulated signal.

In the same field of endeavor, however, Naruse discloses said finger circuit (figure 1) includes a PN sequence generator (figure 2 element 54) having the initial phase set from said searcher and generating the PN code (col 16 lines 10 – 13); a multiplier (figure 2 element 53) for multiplying input reception data (figure 2 element 52) with the PN sequence from said PN sequence generator (figure 2 element 54); and a low-pass filter (figure 2 element 56) for smoothing an output of said multiplier to output a demodulated signal (where the band pass filter is interpreted as a low pass filter because it is inherent that a band pass filter comprises of a low pass filter).

Therefore it would have been obvious to one skilled in the art at the time of invention was made that said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code; a multiplier for multiplying input reception data with the PN sequence from said PN sequence generator; and a low-pass filter for smoothing an output of said multiplier to output a demodulated signal as taught by Naruse in the system of Wang RAKE reception apparatus to alleviate the fading due to the multi-paths and to improve signal to noise ratio to provide a cleaner signal.

32. Regarding claim 19, Wang discloses all limitations of claim 19 as analyzed in claim 12 above. Miura further discloses a The RAKE reception apparatus wherein a value of the shift register constituting the PN sequence generator of the selected finger circuit is supplied through said changeover circuit to said DLL circuit (col 3 lines 58 – 67). However Wang does not disclose said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code; a multiplier for multiplying input reception data with the PN sequence from said PN sequence generator; and a low-pass filter for smoothing an output of said multiplier to output a demodulated signal.

In the same field of endeavor, however, Naruse discloses said finger circuit (figure 1) includes a PN sequence generator (figure 2 element 54) having the initial phase set from said searcher and generating the PN code (col 16 lines 10 – 13); a multiplier (figure 2 element 53) for multiplying input reception data (figure 2 element 52) with the PN sequence from said PN sequence generator (figure 2 element 54); and a

low-pass filter (figure 2 element 56) for smoothing an output of said multiplier to output a demodulated signal (where the band pass filter is interpreted as a low pass filter because it is inherent that a band pass filter comprises of a low pass filter).

Therefore it would have been obvious to one skilled in the art at the time of invention was made that said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code; a multiplier for multiplying input reception data with the PN sequence from said PN sequence generator; and a low-pass filter for smoothing an output of said multiplier to output a demodulated signal as taught by Naruse in the system of Wang RAKE reception apparatus to alleviate the fading due to the multi-paths and to improve signal to noise ratio to provide a cleaner signal.

33. Regarding claim 20, Wang discloses all limitations of claim 20 as analyzed in claim 17 above. Miura further discloses a The RAKE reception apparatus wherein a value of the shift register constituting the PN sequence generator of the selected finger circuit is supplied through said changeover circuit to said DLL circuit (col 3 lines 58 – 67). Naruse further discloses said finger circuit (figure 1) includes a PN sequence generator (figure 2 element 54) having the initial phase set from said searcher and generating the PN code (col 16 lines 10 – 13); a multiplier (figure 2 element 53) for multiplying input reception data (figure 2 element 52) with the PN sequence from said PN sequence generator (figure 2 element 54); and a low-pass filter (figure 2 element 56) for smoothing an output of said multiplier to output a demodulated signal (where the

band pass filter is interpreted as a low pass filter because it is inherent that a band pass filter comprises of a low pass filter).

34. Regarding claim 21, Wang discloses all limitations of claim 21 as analyzed in claim 7 above. Wang further discloses a RAKE reception apparatus in which said DLL circuit (figure 2 element 22) includes first and second multipliers (figure 3 elements 152 and 158) for being fed with an early PN code and a late PN code output (figure 4B output of elements 60 and 62) from the one finger circuit selected by said changeover circuit and for multiplying the reception data with said early PN code and said late PN code (figure 2 elements RI, RQ, and 9); a loop filter for smoothing an output of said subtractor (col 5 lines 55 – 58); Miura further discloses a voltage-controlled oscillator for being fed with an output (figure 1 element 104); wherein output clocks of said voltage-controlled oscillator (figure 1 element 104) is fed to said respective finger circuits (figure 1 plurality of elements 101). However Wnag does not disclose that first and second filters for being fed with outputs of said first and second multipliers, respectively; first and second detectors for detecting outputs of said first and second filters, respectively; a subtractor for subtracting an output of said second detector from an output of said first detector; and a voltage-controlled oscillator for being fed with an output of said loop filter as a control voltage.

In the same field of endeavor, however, Naruse discloses first and second filters for being fed with outputs of said first and second multipliers, respectively (figure 6 elements 87 and 88); first and second detectors for detecting outputs of said first and second filters, respectively (figure 6 elements 89 and 90); a subtractor for subtracting an

output of said second detector from an output of said first detector (figure 6 element 91); and a voltage-controlled oscillator for being fed with an output of said loop filter as a control voltage (figure 6 elements 75 and 92, where element 75 is interpreted as Miura's controller).

Therefore it would have been obvious to one skilled in the art at the time of invention was made that first and second filters for being fed with outputs of said first and second multipliers, respectively; first and second detectors for detecting outputs of said first and second filters, respectively; a subtractor for subtracting an output of said second detector from an output of said first detector; and a voltage-controlled oscillator for being fed with an output of said loop filter as a control voltage as taught by Naruse in the system of Wang RAKE reception apparatus to alleviate the fading due to the multi-paths and to improve signal to noise ratio to provide a cleaner signal.

35. Regarding claim 22, Wang discloses all limitations of claim 22 as analyzed in claim 7 above. Wang further discloses a RAKE reception apparatus wherein said PN sequence generator (figure 2 element 24) is configured for generating an early PN code preceding the PN code in timing (figure 4B output of element 60) and a late PN code later in timing than the PN code (figure 4B output of element 62) used in said finger circuit, and for outputting the early and late PN codes to said changeover circuit (col 1 lines 48 – 54 and col 4 lines 46 – 60). However, Wang does not disclose wherein said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code; a multiplier for multiplying input reception data

with the PN sequence from said PN sequence generator; and a low-pass filter for smoothing an output of said multiplier to output a demodulated signal.

In the same field of endeavor, however, Naruse discloses said finger circuit (figure 1) includes a PN sequence generator (figure 2 element 54) having the initial phase set from said searcher and generating the PN code (col 16 lines 10 – 13); a multiplier (figure 2 element 53) for multiplying input reception data (figure 2 element 52) with the PN sequence from said PN sequence generator (figure 2 element 54); and a low-pass filter (figure 2 element 56) for smoothing an output of said multiplier to output a demodulated signal (where the band pass filter is interpreted as a low pass filter because it is inherent that a band pass filter comprises of a low pass filter).

Therefore it would have been obvious to one skilled in the art at the time of invention was made that said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code; a multiplier for multiplying input reception data with the PN sequence from said PN sequence generator; and a low-pass filter for smoothing an output of said multiplier to output a demodulated signal as taught by Naruse in the system of Wang RAKE reception apparatus to alleviate the fading due to the multi-paths and to improve signal to noise ratio to provide a cleaner signal.

36. Regarding claim 23, Wang discloses all limitations of claim 23 as analyzed in claim 21 above. Wang further discloses a RAKE reception apparatus wherein said PN sequence generator (figure 2 element 24) is configured for generating an early PN code preceding the PN code in timing (figure 4B output of element 60) and a late PN code

later in timing than the PN code (figure 4B output of element 62) used in said finger circuit, and for outputting the early and late PN codes to said changeover circuit (col 1 lines 48 – 54 and col 4 lines 46 – 60). However, Wang does not disclose wherein said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code; a multiplier for multiplying input reception data with the PN sequence from said PN sequence generator; and a low-pass filter for smoothing an output of said multiplier to output a demodulated signal.

In the same field of endeavor, however, Naruse discloses said finger circuit (figure 1) includes a PN sequence generator (figure 2 element 54) having the initial phase set from said searcher and generating the PN code (col 16 lines 10 – 13); a multiplier (figure 2 element 53) for multiplying input reception data (figure 2 element 52) with the PN sequence from said PN sequence generator (figure 2 element 54); and a low-pass filter (figure 2 element 56) for smoothing an output of said multiplier to output a demodulated signal (where the band pass filter is interpreted as a low pass filter because it is inherent that a band pass filter comprises of a low pass filter).

Therefore it would have been obvious to one skilled in the art at the time of invention was made that said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code; a multiplier for multiplying input reception data with the PN sequence from said PN sequence generator; and a low-pass filter for smoothing an output of said multiplier to output a demodulated signal as taught by Naruse in the system of Wang RAKE reception

apparatus to alleviate the fading due to the multi-paths and to improve signal to noise ratio to provide a cleaner signal.

37. Regarding claim 24, Wang discloses all limitations of claim 24 as analyzed in claim 7 above. Wang further discloses a RAKE reception apparatus wherein PN codes having an in-phase component PNI (figure 3 element PNI) and a quadrature component PNQ (figure 3 element PNQ); a complex multiplier (Figure 3 elements 152, 154, 156, and 158) for multiplying received input in-phase (I)/quadrature (Q) data (figure 3 elements RI and RQ) with the PN sequence (PNI, PNQ) (figure 3 elements PNI and PNQ) from said PN sequence generator (Figure 2 element 24). However, Wang does not disclose said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating PN codes; and a low-pass filter for smoothing an output of said complex multiplier for outputting a demodulated signal.

In the same field of endeavor, however, Naruse discloses said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating PN codes (col 16 lines 10 – 13); and a low-pass filter (figure 2 element 56) for smoothing an output of said multiplier to output a demodulated signal (where the band pass filter is interpreted as a low pass filter because it is inherent that a band pass filter comprises of a low pass filter).

Therefore it would have been obvious to one skilled in the art at the time of invention was made that said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating PN codes; and a low-pass filter for smoothing an output of said complex multiplier for outputting a demodulated signal

as taught by Naruse in the system of Wang RAKE reception apparatus to alleviate the fading due to the multi-paths and to improve signal to noise ratio to provide a cleaner signal.

38. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 6266365) in view of Miura (US 6658046), in further view of Naruse (US 6075809) and in further view of Saito (US 6081548).

Regarding claim 25, Wang discloses all limitations of claim 25 as analyzed in claim 7 above. Wang further discloses a RAKE reception apparatus wherein said DLL circuit (figure 2 element 22) includes a PN sequence generator (figure 2 element 24) for generating and outputting early PN codes (figure 4B output of element 60) (an in-phase component PNI (figure 4B element CIEI) and a quadrature component PNQ(figure 4B element CIEQ)) earlier in timing than the PN codes used in said finger circuit (an in-phase component PNI (figure 3 element PNI) and a quadrature component PNQ (figure 4B element PNQ)) and for generating and outputting late PN codes (figure 4B output of element 62) (an in-phase component PNLI (figure 4B element CILI) and a quadrature component PNLQ (figure 4B element CILQ)) later in timing than the PN codes used in said finger circuit (an in-phase component PNI (figure 3 element PNI) and a quadrature component PNQ (figure 3 element PNQ)); and a loop filter for smoothing an output of said subtractor (figure 6 element 92). Miura discloses a voltage-controlled oscillator fed with an output (figure 1 element 104); wherein a value of a shift register of a PN sequence generator of said one finger circuit selected through said changeover circuit is loaded in the shift register of said PN sequence generator (figure 1 element 101, 107,

and 108); and wherein output clocks of said voltage-controlled oscillator (figure 1 element 104) are routed to said PN sequence generator (figure 1 element 108) and to said respective finger circuits (figure 1 plurality of elements 101). However, Wang does not disclose a first complex multiplier for multiplying received in-phase (I) and quadrature (Q) data with the PN codes (PNEI, PNEQ) generated by said PN sequence generator; a second complex multiplier for multiplying received in-phase (I) and quadrature (Q) data with the PN codes (PNLI, PNLQ) generated by said PN sequence generator; a first low-pass filter for smoothing an output of said first complex multiplier; a second low-pass filter for smoothing an output of said second complex multiplier; a first amplitude detector for detecting an output amplitude of said first low-pass filter; a second amplitude detector for detecting an output amplitude of said second low-pass filter; a subtractor for subtracting an output of said second amplitude detector from an output of said first amplitude detector; and a voltage-controlled oscillator fed with an output of said subtractor as a control voltage;

In the same field of endeavor, however, Naruse discloses a first low-pass filter (figure 6 element 87 where the band pass filter is interpreted as a low pass filter because it is inherent that a band pass filter comprises of a low pass filter) for smoothing an output of said first complex multiplier (figure 6 element 79); a second low-pass filter (figure 6 element 88 where the band pass filter is interpreted as a low pass filter because it is inherent that a band pass filter comprises of a low pass filter) for smoothing an output of said second complex multiplier (figure 6 element 80); a first amplitude detector (figure 6 element 89) for detecting an output amplitude of said first

low-pass filter (figure 6 element 87); a second amplitude detector (figure 6 element 90) for detecting an output amplitude of said second low-pass filter (figure 6 element 88); a subtractor (figure 6 element 91) for subtracting an output of said second amplitude detector from an output of said first amplitude detector; and a voltage-controlled oscillator fed with an output of said subtractor as a control voltage (figure 6 element 75 and 92 where element 75 is interpreted as Miura's controller);

Also in the same field of endeavor, however, Saito discloses a first complex multiplier (figure 2 element 31) for multiplying received in-phase (I) and quadrature (Q) data (figure 2 element received signal where received signal is interpreted as the received signal in Wang's system which is made up of I and Q data) with the PN codes (PNEI, PNEQ) (figure 2 element PN code early) generated by said PN sequence generator (figure 2 element 40 and col 7 line 17); a second complex multiplier (figure 2 element 32) for multiplying received in-phase (I) and quadrature (Q) data (figure 2 element received signal where received signal is interpreted as the received signal in Wang's system which is made up of I and Q data) with the PN codes (PNLI, PNLQ) (figure 2 element PN code late) generated by said PN sequence generator (figure 2 element 40 and col 7 line 17).

Therefore it would have been obvious to one skilled in the art at the time of invention was made that a first low-pass filter for smoothing an output of said first complex multiplier; a second low-pass filter for smoothing an output of said second complex multiplier; a first amplitude detector for detecting an output amplitude of said first low-pass filter; a second amplitude detector for detecting an output amplitude of

said second low-pass filter; a subtractor for subtracting an output of said second amplitude detector from an output of said first amplitude detector; and a voltage-controlled oscillator fed with an output of said subtractor as a control voltage as taught by Naruse in the system of Wang RAKE reception apparatus to alleviate the fading due to the multi-paths and to improve signal to noise ratio to provide a cleaner signal and a first complex multiplier for multiplying received in-phase (I) and quadrature (Q) data with the PN codes (PNEI, PNEQ) generated by said PN sequence generator; a second complex multiplier for multiplying received in-phase (I) and quadrature (Q) data with the PN codes (PNLI, PNLQ) generated by said PN sequence generator as taught by Saito in the system of Wang RAKE reception apparatus to improve the communication quality and reduce the power consumption.

Allowable Subject Matter

39. Claims 26 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other prior art cited

The prior art made of record and not relies upon is considered pertinent to applicant's disclosure.

40. Naruse et al. (US 6072822) discloses a fingered reception apparatus. Some components include: a searcher, a pll, a controller, filters, a PN generator, multipliers, a subtractor and detectors.

41. Naruse (US 6389060) discloses a fingered reception apparatus. Some components include: a searcher, a pll, a controller, filters, a PN generator, multipliers, a subtractor and detectors.

42. Garyantes (US 6463048) discloses an apparatus that has a multipliers multiplying the received signal with an early and late signal.

Contact information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aslan Ettehadieh whose telephone number is (571) 272-8729. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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